WHAT IS CLAIMED IS:

1. An floating gate transistor, comprising:

a channel island region;

a source region located adjacent to a first side of the channel island region;

a drain region located adjacent to a second side of the channel island region;

a tunneling dielectric located above the channel island region;

a floating gate having a first, second, third and fourth side surfaces, wherein the floating gate is located above the tunneling dielectric;

a control gate dielectric located above the floating gate;

a control gate located above the control gate dielectric; and

wherein first and second side surfaces of the control gate are aligned to third and fourth side surfaces of the channel island region, and to the third and the fourth side surfaces of the floating gate.

2. The transistor of claim 1, wherein the first and the second side surfaces of the control gate are aligned to side surfaces of the control gate dielectric and to side surfaces of the tunneling dielectric.

3. The transistor of claim 1, wherein:

the control gate dielectric is located on a top surface of the floating gate and on upper portions of the first and the second side surfaces of the floating gate; and

the control gate is located on the control gate dielectric above a top surface of the floating gate and laterally adjacent to the upper portions of the first and the second side surfaces of the floating gate.

4. The transistor of claim 3, wherein the control gate comprises a portion of a word line that extends in a direction substantially parallel to a source–channel–drain direction of the transistor.

5. The transistor of claim 4, further comprising:

an intergate insulating layer located above the source and drain regions, laterally adjacent to lower portions of the first and the second side surfaces of the floating gate and below a bottom surface of the control gate;

a first bit line contacting the source region; and

a second bit line contacting the drain region.

6. The transistor of claim 5, wherein the first and the second bit lines are located under the intergate insulating layer, and extend in a direction substantially perpendicular to the source-channel-drain direction.

7. The transistor of claim 6, further comprising:

sidewall spacers located between the intergate insulating layer and the lower portions of the first and the second side surfaces of the floating gate; and

metal silicide regions contacting the bit lines.

8. The transistor of claim 7, wherein the source and the drain regions comprise a heavily doped portion and a lightly doped portion.

9. The transistor of claim 1, wherein the source and the drain regions are located asymmetrically with respect to the floating gate.

10. The transistor of claim 1, wherein the transistor is formed using two photolithographic masking steps.

11. The transistor of claim 1, wherein:

the source, the drain and the channel island region are formed in a polysilicon active layer, which is located above a substrate; and

the transistor comprises a TFT EEPROM.

12. A three dimensional nonvolatile memory array, comprising:

a plurality of vertically separated device levels, each level comprising an array of TFT EEPROMs of claim 11;

a plurality of bit line columns in each device level, each bit line contacting the source or the drain regions of the TFT EEPROMs;

a plurality of word line rows in each device level; and

at least one interlayer insulating layer located between the device levels.

13. The array of claim 12, wherein:

the columns of bit lines extend substantially perpendicular to a source-channel-drain direction of the TFT EEPROMs;

each word line contains the control gates of the TFT EEPROMs, and the rows of word lines extend substantially parallel to the source-channel-drain direction of the TFT EEPROMs; and

the floating gates of the TFT EEPROMs comprise posts located between the control gates, the channel region islands and an intergate insulating layer.

14. The array of claim 13, wherein the bit lines in each device level comprise rails which extend under the intergate insulating layer.

15. The array of claim 14, wherein:

the rails comprise silicide layers over doped semiconductor regions;

the doped semiconductor regions comprise the TFT EEPROM source and drain regions in areas where the doped semiconductor regions are located adjacent to the TFT EEPROM channels; and

the array comprises a NVG, a DuSNOR or a SSL-NOR three dimensional array.

16. The array of claim 12, further comprising an interlevel interconnect which connects devices on different device levels, wherein at least a portion of the word line row comprises the same layer as the interlevel interconnect.

17. The array of claim 12, further comprising an insulating fill layer located between adjacent rail stacks, the rail stacks comprising the control gate, the control gate dielectric, the floating gate, the tunnel dielectric and the channel island region.

18. A method of making a floating gate transistor, comprising:

providing a semiconductor active area;

forming a tunnel dielectric layer over the active area;

forming a floating gate layer over the tunnel dielectric layer;

forming a first photoresist mask over the floating gate layer;

patterning the floating gate layer using the first photoresist mask to form a floating gate rail;

doping the active area using the floating gate rail as a mask to form source and drain regions in the active area;

forming an intergate insulating layer adjacent to lower portions of side surfaces of the floating gate rail;

forming a control gate dielectric layer over and adjacent to upper portions of the side surfaces of the floating gate rail;

forming a control gate layer over the control gate dielectric layer;

forming a second photoresist mask over the control gate layer; and

patterning the control gate layer, the control gate dielectric layer, the floating gate rail, the tunnel dielectric layer and the active area using the second photoresist mask to form a control gate, a control gate dielectric, a floating gate, a tunnel dielectric and a channel island region.

19. The method of claim 18, comprising forming the entire floating gate transistor using two photolithographic masking steps.

20. The method of claim 18, wherein forming an intergate insulating layer adjacent to the side surfaces of the floating gate rail comprises:

forming the intergate insulating layer over and adjacent to the floating gate rail; and

etching back the intergate insulating layer such that the intergate insulating layer remains adjacent to the lower portions of the floating gate rail side surfaces below the upper portions of the floating gate rail side surfaces.

21. The method of claim 20, further comprising:

forming a hardmask over the floating gate layer;

forming the first photoresist mask on the hardmask layer; and

patterning the hardmask layer and the floating gate layer using the first photoresist mask to form a first rail stack comprising a hardmask rail and the floating gate rail.

22. The method of claim 21, further comprising:

implanting lightly doped portions of the source and drain regions using the first rail stack as a mask;

forming sidewall spacers on the first rail stack;

implanting heavily doped portions of the source and drain regions using the first rail stack and the sidewall spacers as a mask;

forming a metal layer over the source and drain regions and over the first rail stack;

annealing the first metal layer to react the metal layer with the source and drain regions to selectively form metal silicide regions on the source and drain regions; and

selectively etching the unreacted metal layer remaining on the sidewall spacers and the first rail stack.

23. The method of claim 22, further comprising:

selectively removing the hardmask and sidewall spacers from upper portions of the floating gate rail;

forming the control gate dielectric layer on the upper portions of the side surfaces of the floating gate rail and on the top surface of the floating gate rail; and

forming the control gate layer on the control gate dielectric layer such that the control gate layer is located over the top surface of the floating gate rail and laterally adjacent to the upper portions of the side surfaces of the floating gate rail.

24. The method of claim 23, further comprising roughening the top surface and the upper portions of the side surfaces of the floating gate rail prior to forming the control gate dielectric layer.

25. The method of claim 21, wherein forming the source and drain regions comprises performing an angled implant using the first rail stack as a mask to form source and drain regions which are asymmetric with respect to the first rail stack.

26. The method of claim 25, wherein the angled implant comprises implanting heavily doped source and drain regions.

27. The method of claim 26, further comprising implanting a lightly doped portion of the source region perpendicular to the active area.

28. The method of claim 18, further comprising:

patterning the floating gate layer using the first photoresist mask to form a plurality of floating gate rails;

doping the active area using the floating gate rails as a mask to form a plurality of source and drain regions in the active area;

forming the intergate insulating layer between lower portions of the side surfaces of the floating gate rails;

forming the control gate dielectric layer and the control gate layer over and adjacent to upper portions of the side surfaces of the floating gate rails;

forming the second photoresist mask over the control gate layer; and

patterning the control gate layer, the control gate dielectric layer, the floating gate rails, the tunnel dielectric layer and the active area using the second photoresist mask to form a plurality of control gates, a plurality of control gate dielectrics, a plurality of floating gates, a plurality of tunnel dielectrics and a plurality of channel island regions.

29. The method of claim 28, wherein the intergate insulating layer protects the plurality of source and drain regions in the active area during the patterning of the floating gate rails and the active area.

30. The method of claim 28, further comprising forming an insulating fill layer between adjacent second rail stacks, wherein each second rail

stack comprises one of the plurality of control gates, one the plurality of control gate dielectrics, one of the plurality of floating gates, one of the plurality of tunnel dielectrics and one of the plurality of channel island regions.

31. The method of claim 28, wherein forming an intergate insulating layer adjacent to the side surfaces of the floating gate rail comprises:

forming the intergate insulating layer over and adjacent to the floating gate rails; and

etching back the intergate insulating layer such that the intergate insulating layer remains between the floating gate rails, adjacent to the lower portions of the floating gate rail side surfaces below the upper portions of the floating gate rail side surfaces.

32. The method of claim 31, further comprising patterning the hardmask layer and the floating gate layer using the first photoresist mask to form a plurality of first rail stacks each comprising a hardmask rail and the floating gate rail.

33. The method of claim 32, further comprising:

implanting a plurality of lightly doped portions of the source and drain regions using the first rail stacks as a mask;

forming sidewall spacers on the first rail stacks;

implanting a plurality of heavily doped portions of the source and drain regions using the first rail stacks and the sidewall spacers as a mask;

forming a metal layer over the plurality of source and drain regions and over the first rail stacks;

annealing the first metal layer to react the metal layer with the plurality of source and drain regions to selectively form metal silicide regions on the plurality of source and drain regions; and

selectively etching the unreacted metal layer remaining on the sidewall spacers and the first rail stacks.

34. The method of claim 33, further comprising:

selectively removing the hardmask and sidewall spacers from upper portions of the floating gate rails;

forming the control gate dielectric layer on the upper portions of the side surfaces of the floating gate rails and on the top surface of the floating gate rails; and

forming the control gate layer on the control gate dielectric layer such that the control gate layer is located over the top surface of the floating gate rails and laterally adjacent to the upper portions of the side surfaces of the floating gate rails.

35. The method of claim 34, further comprising patterning the active area using a third mask to form a plurality of islands containing two EEPROM transistors sharing a common source to form a DuSNOR array.

36. The method of claim 34, further comprising patterning the active area using a third mask to form a plurality of islands containing one EEPROM transistor to form a SSL-NOR array with separated drain and source lines.

37. The method of claim 34, wherein:

the step of doping the active area further comprises forming a plurality of bit lines containing the plurality of source and drain regions,

wherein the bit lines extend substantially perpendicular to a source-channel-drain direction;

the step of forming metal silicide regions comprises forming a metal silicide on the plurality of bit lines; and

the step of patterning the active area comprises etching the active area to form a plurality of channel island regions without etching the bit lines containing the source and drain regions which are covered by the intergate insulating layer.

38. The method of claim 18, wherein providing the semiconductor active area comprises forming a polysilicon active layer over an interlayer insulating layer.

39. The method of claim 38, wherein:

forming the tunnel dielectric layer over the active area comprises growing a thermal silicon oxide layer on the polysilicon active layer;

forming the floating gate layer over the tunnel dielectric layer comprises forming a polysilicon layer on the tunnel dielectric layer;

forming the first photoresist mask over the floating gate layer comprises forming the photoresist on a hardmask layer located on the floating gate layer;

patterning the floating gate layer using the first photoresist mask to form a floating gate rail comprises anisotropically etching the hardmask layer and the floating gate layer during one etching step using the first photoresist mask;

doping the active area using the floating gate rail as a mask to form source and drain regions in the active area comprises ion implanting the source and drain regions using the floating gate rail as a mask;

forming the intergate insulating layer adjacent to the side surfaces of the floating gate rail comprises forming the intergate insulating layer

over and adjacent to the floating gate rail and etching back the intergate insulating layer such that the intergate insulating layer remains adjacent to the lower portions of the floating gate rail side surfaces below the upper portions of the floating gate rail side surfaces;

forming the control gate dielectric layer comprises growing a thermal silicon oxide layer on the floating gate rail, depositing a silicon nitride layer on the thermal silicon oxide layer and depositing a silicon oxide layer on the silicon nitride layer;

forming the control gate layer over the control gate dielectric layer comprises depositing a polysilicon layer and a silicide layer on the control gate dielectric layer;

forming the second photoresist mask over the control gate layer comprises forming the second photoresist mask on the control gate layer; and

patterning the control gate layer, the control gate dielectric layer, the floating gate rail, the tunnel dielectric layer and the active area using the second photoresist mask comprises anisotropically etching the control gate layer, the control gate dielectric layer, the floating gate rail, the tunnel dielectric layer and the active layer in one etching step to form second rail stacks.

40. The method of claim 28, further comprising:

forming an interlayer insulating layer below the active area;

forming at least one via extending through the interlayer insulating layer to a lower device level or to a driver circuit in a substrate;

depositing at least a portion of the control gate layer in the at least one via; and

patterning the control gate layer to form the plurality of control gates and an interlevel interconnect which connects the floating gate

transistor with a device on a lower device level or with a driver circuit in the substrate.

41. The method of claim 40, further comprising:

forming a heavily doped polysilicon layer comprising a lower portion of the control gate layer;

forming the at least one via extending through the heavily doped polysilicon layer;

forming a conductive layer comprising an upper portion of the control gate layer on the heavily doped polysilicon layer and in the at least one via; and

patterning the heavily doped polysilicon layer and the conductive layer to form the plurality of control gates and the interlevel interconnect.

42. A method of forming a monolithic three dimensional memory array, comprising:

providing a first array of transistors of claim 28;

forming an interlayer insulating layer over the array; and

monolithically forming at least a second array of TFT EEPROMs on the interlayer insulating layer.

43. A method of forming a three dimensional memory array, comprising:

providing a plurality of arrays of transistors of claim 28 on different silicon on insulator substrates;

thinning the substrates; and

attaching the arrays to each other to form a three dimensional memory array.

44. A method of claim 25, further comprising:

programming the floating gate EEPROM transistor by Fowler-Nordheim electron tunneling from the floating gate to the drain region; and

erasing the floating gate EEPROM transistor by Fowler-Nordheim electron tunneling from the channel island region to the floating gate.

45. A method of forming an array of floating gate transistors, comprising:

forming at least portions of a plurality of floating gates over a tunnel dielectric located over a semiconductor active area;

doping the active area using the at least portions of the plurality of floating gates as a mask to form a plurality of bit lines in the active area;

forming an intergate insulating layer between lower portions of side surfaces of the at least portions of the plurality of floating gates;

forming a control gate dielectric on exposed upper surfaces of the at least portions of the floating gates and on exposed upper portions of side surfaces of the at least portions of the floating gates; and

forming a plurality of word lines over the control dielectric and over the intergate insulating layer.

46. The method of claim 45, further comprising:

providing the semiconductor active area;

forming a tunnel dielectric layer over the active area;

forming a floating gate layer over the tunnel dielectric layer;

forming a first photoresist mask over the floating gate layer;

patterning the floating gate layer using the first photoresist mask to form the plurality of the floating gate portions comprising floating gate rails;

doping the active area using the floating gate rails as a mask to form the plurality of bit lines containing transistor source and drain regions;

forming a control gate dielectric layer and a control gate layer over and adjacent to upper portions of the side surfaces of the floating gate rails;

forming a second photoresist mask over the control gate layer; and

patterning the control gate layer, the control gate dielectric layer, the floating gate rails, the tunnel dielectric layer and the active area using the second photoresist mask to form the plurality of word lines containing transistor control gates, a plurality of control gate dielectrics, a plurality of floating gates, a plurality of tunnel dielectrics and a plurality of channel island regions.

47. The method of claim 46, wherein forming the intergate insulating layer comprises:

forming the intergate insulating layer over and adjacent to the floating gate rails; and

etching back the intergate insulating layer such that the intergate insulating layer remains between the floating gate rails, adjacent to the lower portions of the floating gate rail side surfaces below the upper portions of the floating gate rail side surfaces.

48. The method of claim 47, further comprising:

forming a hardmask layer over the floating gate layer; and

patterning the hardmask layer and the floating gate layer using the first photoresist mask to form a plurality of first rail stacks each comprising a hardmask rail and the floating gate rail.

49. The method of claim 48, further comprising forming an insulating fill layer between adjacent second rail stacks, wherein each second rail stack comprises one of the plurality of word lines, one the plurality of control gate dielectrics, one of the plurality of floating gates, one of the plurality of tunnel dielectrics and one of the plurality of channel island regions.

50. The method of claim 49, further comprising:

implanting a plurality of lightly doped portions of the source and drain regions using the first rail stacks as a mask;

forming sidewall spacers on the first rail stacks;

implanting a plurality of heavily doped portions of the source and drain regions using the first rail stacks and the sidewall spacers as a mask;

forming a metal layer over the plurality of bit lines, over the plurality of source and drain regions and over the first rail stacks;

annealing the first metal layer to react the metal layer with the plurality of bit lines and the plurality of source and drain regions to selectively form metal silicide regions on the plurality of bit lines and the plurality of source and drain regions; and

selectively etching the unreacted metal layer remaining on the sidewall spacers and the first rail stacks.

51. The method of claim 50, wherein:

providing the semiconductor active area comprises forming a polysilicon active layer over an interlayer insulating layer;

forming the tunnel dielectric layer over the active area comprises growing a thermal silicon oxide layer on the polysilicon active layer;

forming the floating gate layer over the tunnel dielectric layer comprises forming a polysilicon layer on the tunnel dielectric layer;

forming the first photoresist mask over the floating gate layer comprises forming the photoresist on the hardmask layer;

patterning the floating gate layer using the first photoresist mask to form a floating gate rail comprises anisotropically etching the hardmask layer and the floating gate layer during one etching step using the first photoresist mask;

forming the control gate dielectric layer comprises growing a thermal silicon oxide layer on the floating gate rail, depositing a silicon nitride layer on the thermal silicon oxide layer and depositing a silicon oxide layer on the silicon nitride layer;

forming the control gate layer over the control gate dielectric layer comprises depositing a polysilicon layer and a silicide layer on the control gate dielectric layer;

forming the second photoresist mask over the control gate layer comprises forming the second photoresist mask on the control gate layer; and

patterning the control gate layer, the control gate dielectric layer, the floating gate rail, the tunnel dielectric layer and the active area using the second photoresist mask comprises anisotropically etching the control gate layer, the control gate dielectric layer, the floating gate rail, the tunnel dielectric layer and the active layer in one etching step to form the second rail stacks.

52. A method of forming a monolithic three dimensional memory array, comprising:

providing a first array of floating gate EEPROM transistors of claim 45;

forming an interlayer insulating layer over the array; and

monolithically forming at least a second array of TFT EEPROMs on the interlayer insulating layer.

53. A method of forming a three dimensional memory array, comprising:

providing a plurality of arrays of floating gate EEPROM transistors of claim 45 on different silicon on insulator substrates;

thinning the substrates; and

attaching the arrays to each other to form a three dimensional memory array.

54. The method of claim 45, further comprising:

forming an interlayer insulating layer below the active area;

forming at least one via extending through the interlayer insulating layer to a lower device level or to a driver circuit in a substrate;

depositing at least a portion of a word line layer in the at least one via; and

patterning the word line layer to form the plurality of word lines and an interlevel interconnect which connects the array of transistors with a device on a lower device level or with a driver circuit in the substrate.

55. The method of claim 54, further comprising:

forming a heavily doped polysilicon layer comprising a lower portion of the word line layer;

forming the at least one via extending through the heavily doped polysilicon layer;

forming a conductive layer comprising an upper portion of the word line layer on the heavily doped polysilicon layer and in the at least one via; and

patterning the heavily doped polysilicon layer and the conductive layer to form the plurality of word lines and the interlevel interconnect.

56. A method of making a floating gate transistor, comprising forming the entire floating gate transistor using two photolithographic masking steps.

57. The method of claim 56, further comprising:

providing a semiconductor active area;

forming a tunnel dielectric layer over the active area;

forming a floating gate layer over the tunnel dielectric layer;

forming a first photoresist mask over the floating gate layer in a first photolithographic masking step;

patterning the floating gate layer using the first photoresist mask to form a floating gate rail;

doping the active area using the floating gate rail as a mask to form source and drain regions in the active area;

forming an intergate insulating layer adjacent to lower portions of side surfaces of the floating gate rail;

forming a control gate dielectric layer over and adjacent to upper portions of the side surfaces of the floating gate rail;

forming a control gate layer over the control gate dielectric layer;

forming a second photoresist mask over the control gate layer in a second photolithographic masking step; and

patterning the control gate layer, the control gate dielectric layer, the floating gate rail, the tunnel dielectric layer and the active area using the second photoresist mask to form a control gate, a control gate dielectric, a floating gate, a tunnel dielectric and a channel island region.

58. The method of claim 57, wherein forming an intergate insulating layer adjacent to the side surfaces of the floating gate rail comprises:

forming the intergate insulating layer over and adjacent to the floating gate rail; and

etching back the intergate insulating layer such that the intergate insulating layer remains adjacent to the lower portions of the floating gate rail side surfaces below the upper portions of the floating gate rail side surfaces.

59. The method of claim 58, further comprising:

forming a hardmask over the floating gate layer;

forming the first photoresist mask on the hardmask layer;

patterning the hardmask layer and the floating gate layer using the first photoresist mask to form a first rail stack comprising a hardmask rail and the floating gate rail;

implanting lightly doped portions of the source and drain regions using the first rail stack as a mask;

forming sidewall spacers on the first rail stack;

implanting heavily doped portions of the source and drain regions using the first rail stack and the sidewall spacers as a mask;

forming a metal layer over the source and drain regions and over the first rail stack;

annealing the first metal layer to react the metal layer with the source and drain regions to selectively form metal silicide regions on the source and drain regions; and

selectively etching the unreacted metal layer remaining on the sidewall spacers and the first rail stack.

60. The method of claim 59, further comprising:

selectively removing the hardmask and sidewall spacers from upper portions of the floating gate rail;

forming the control gate dielectric layer on the upper portions of the side surfaces of the floating gate rail and on the top surface of the floating gate rail; and

forming the control gate layer on the control gate dielectric layer such that the control gate layer is located over the top surface of the floating gate rail and laterally adjacent to the upper portions of the side surfaces of the floating gate rail.

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